CLAIMS

What is claimed is:

1. A method for monitoring and improving a fabrication process for integrated circuits comprising:

instantiating a test pattern on a plurality of configurable devices fabricated on a wafer using the fabrication process;

identifying at least one underperforming region in at least one of the plurality of configurable devices;

determining if the at least one underperforming region is layout sensitive; and

responsive to the step of determining, adjusting at least one of layout of the at least one of the plurality of configurable devices and the fabrication process.

2. The method of claim 1 further comprising:

dividing each of the plurality of configurable devices into a plurality of regions.

3. The method of claim 2 wherein the step of instantiating a test pattern comprises instantiating a same test pattern in each of the plurality of regions.

4. The method of claim 2 wherein the step of determining comprises correlating performance of each of the plurality of regions with layout of the each of the plurality of configurable devices.

5. The method of claim 4 wherein:

if there is a high correlation, adjusting the layout of the at least one of the plurality of configurable devices; and

if there is a low correlation, adjusting the fabrication process.

6. The method of claim 2 wherein:

the step of determining comprises correlating performance of each of the plurality of regions with the wafer;

if there is a low correlation, adjusting the layout of the at least one of the plurality of configurable devices; and

if there is a high correlation, adjusting the fabrication process.

7. The method of claim 1 wherein the test pattern comprises a ring oscillator.

8. The method of claim 7 wherein the step of identifying comprises measuring a frequency of the ring oscillator.

9. The method of claim 1 wherein the step of identifying comprises measuring at least one of frequency, delay, voltage, current, and signal quality of each of the plurality of configurable devices

10. The method of claim 1 further comprising:

tailoring the test pattern to measure performance of interconnections within the plurality of configurable devices.

11. The method of claim 10 wherein tailoring the test pattern comprises tailoring the test pattern to measure performance of a particular layer within the plurality of configurable devices.

12. The method of claim 10 wherein the interconnections are copper metal lines.

13. The method of claim 1 further comprising:

tailoring the test pattern to measure performance of transistors within the plurality of configurable devices.

14. The method of claim 1 further comprising:

applying test vectors to each of the plurality of configurable devices; and

analyzing results based on the step of applying test vectors.

15. The method of claim 1 wherein adjusting the layout of the at least one of the plurality of configurable devices comprises adding dummy metal.

16. The method of claim 1 further comprising:

after the step of adjusting, repeating the steps of instantiating, identifying and determining.

17. The method of claim 1 wherein the test pattern is also used during the normal testing of the plurality of configurable devices.

18. The method of claim 1 wherein the plurality of configurable devices comprises a programmable logic device.

19. The method of claim 18 wherein the programmable logic device is a field programmable logic array.

20. The method of claim 1 further comprising:

after the step of adjusting, fabricating an integrated circuit different from the plurality configurable devices using the fabrication process.

21. A system for monitoring performance of a fabrication process for integrated circuits comprising:

a wafer comprising a plurality of configurable devices;

each of the plurality of configurable devices comprising a plurality of regions; and

a tester coupled to the wafer, the tester configured for instantiating a test pattern in each of the plurality of regions, identifying at least one underperforming region, and determining if the at least one underperforming region is layout sensitive.

22. The system of claim 21 further comprising:

a probe card coupled between the tester and the wafer for interfacing between the tester and the wafer.

23. The system of claim 21 wherein the plurality of configurable devices comprises a programmable logic device.

24. The system of claim 23 wherein the programmable logic device is a field programmable logic array.

25. A system comprising:

means for instantiating a test pattern on a plurality of configurable devices fabricated on a wafer using a fabrication process;

means for identifying at least one underperforming region in at least one of the plurality of configurable devices;

means for determining if the at least one underperforming region is layout sensitive; and

means for adjusting at least one of layout of the at least one of the plurality of configurable devices and the fabrication process, responsive to the means for determining.